SELECTIVE HARMONIC ELIMINATION USING SHUNT HYBRID ACTIVE POWER FILTERS OPERATING AT DIFFERENT SWITCHING FREQUENCIES

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Abstract—Active filtering of electric power has now become a mature technology for harmonic and reactive power compensation in ac networks. This paper proposes a combination of low- and high frequency hybrid active power filter (APF) to operate in parallel for better performance. The individual hybrid Active Power Filter is a series combination of passive filter with the corresponding voltage source inverter. The dc links of both inverters are connected in parallel, and the voltage of this dc link is maintained by the low-frequency inverter (LFI). The low-and high-frequency inverters eliminate lower and higher order harmonics respectively. In addition, it is possible to design the LFI such that it can also compensate the reactive power of the load. The individual passive filter of the hybrid topology is designed to take care of specific order of harmonics that are predominant in the load. In this paper a design for a three phase active power filter use a reduced switch (B4) topology and one cycle control is presented. The B4 topology offers the advantage of reduced cost and bridge losses at the expense of device stress and increased DC-side voltage. This design also provides the advantages associated with one cycle control. The performances of the proposed topology and the controller are examined by MATLAB/SIMULINK-based simulation.

Keywords- Hybrid Active Power Filter (APF), harmonics, passive filter, reduced switch topology**.**

I. INTRODUCTION

With the increasing use of adjustable speed drives, arc furnace, controlled and uncontrolled rectifiers, and other nonlinear loads, the power distribution system is polluted with harmonics. Such harmonics not only create more voltage and current stress but also are responsible for electromagnetic interference, more losses, capacitor failure due to overloading, harmonic resonance, etc. Introduction of strict legislation such as IEEE519 limits the maximum amount of harmonics that a supply system can tolerate for a particular type of load. Therefore, use of active or passive type filters is essential. In addition, the recent thrust on extracting power from wind and photovoltaic (PV) systems calls for extensive studies on power filters to make the renewable energy green and clean (i.e., free from harmonics). Note that for any active power filter (APF), the voltage source inverter (VSI) has to feed the right nature of compensating current. Different methods to predict the compensating current have been proposed. This includes the traditional d-q and p-q-r theory-based approaches and more recently the soft-computing-based techniques.

The controller design is equally important for an improved performance of an APF.A comparative assessment for different type of controllers including multiple rotating integrators, stationary frame generalized integrators, proportional-sinusoidal integrators, and vector proportional-integral controllers are reported. An outer voltage loop and an inner current loop are necessary for implementation of such linear current control scheme. A nonlinear control technique utilizing two inner current loops and an outer dc bus voltage loop is also proposed. The inner and outer loops are decoupled, and the system took about 1.5 cycles for the outer loop to converge.

Passive filters have the advantages of low cost and losses; however, they have the problems of harmonic resonance with the source and/or the load. Moreover, they need to be tuned properly to take care of a wider frequency range. Active filter may completely replace the passive counterpart. This requires higher voltage/current switches for medium/high power applications. Use of hybrid filter, where a lower rating active filter is added in series with the passive filter, has the merit of operating the active filter at a convenient voltage and current. However,

it required a transformer to couple the passive filter with the active filter. Later, the transformer is eliminated and a hybrid combination for application with diode rectifier is developed. The passive filter connected in series is tuned at seventh harmonics and the active filter is operated at a much lower voltage (at 300 V for a 3.3-kV line). Later researchers developed a dual hybrid configuration where the series filters are tuned to eliminate fifth and seventh current harmonics. Reduced switch topologies have the advantages of more reliability and less cost and complexity. Reduced switch APF with one cycle control is also proposed. The third leg of the inverter is eliminated, and the third phase is connected to the midpoint (derived by voltage splitting capacitors) of the dc bus. This topology has the problem of voltage balancing across the dc link capacitors. This is later improved by connecting the where third phase to the negative pole of the dc link.

Hybrid APF with series resonant networks tuned at different harmonic frequencies are reported and extended the application of an APF to PV cells. A different type of hybrid filter is proposed that uses a series passive filter and a thyristor controlled reactor-based variable impedance shunt passive filter to compensate for the harmonics and reactive power. Such systems have relatively poor dynamic performance and are less suitable for highly dynamic types of load. This paper is an integration of passive and active reduced switch filters to optimally compensate the load.
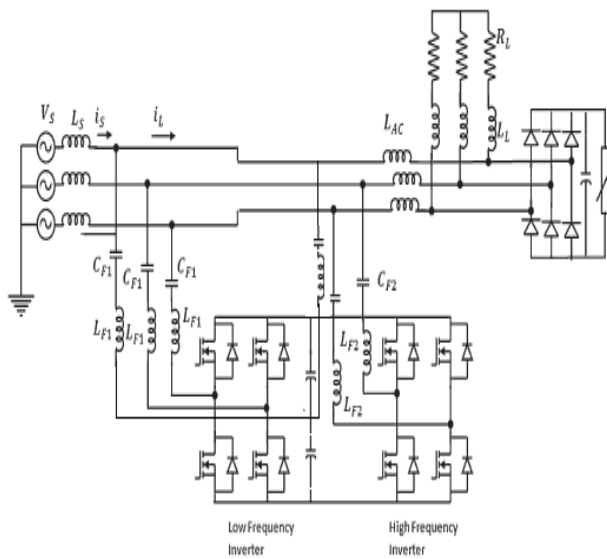

Fig.1. Reduced Switch Dual Parallel Topology

TABLE I
SYSTEM SPECIFICATION

Line Voltage (line-line)	110V
Line frequency	50Hz
Power System Inductance (Ls)	2mH
AC inductor to the rectifier	25mH
DC load side capacitor after rectifier	47µF
DC link voltage	1500V
DC link capacitors C1,C2	3300µF
Switching frequency of inverter1	550Hz
Switching frequency of inverter2	20KHz

II. SYSTEM CONFIGURATION

The topology of the proposed APF is shown in Fig. 1. This is the reduced switch version of the corresponding full-bridge topology. A pair of switches (i.e., one leg) is removed from each of the VSIs of the full-bridge configuration. A diode bridge feeding a resistive load is considered as the nonlinear load for this study. The system consists of a parallel connection of two units. Each unit is a series connection of passive and APF. The two units are optimized to take care of low- and high-frequency components of the load, respectively. The low frequency inverter (LFI) operates at 550 Hz and is connected in series with the passive filter tuned to eliminate optimally the fifth and seventh harmonics. Note that this inverter may also supply the reactive power demand of the load. In such case, the inverter may also operate under the selective harmonic elimination mode removing fifth and seventh harmonics with minimum number of switching per half cycle. The second unit is the high frequency inverter (HFI) operates at 20 kHz and passive filter of the second unit is tuned to optimally eliminate the 11th and 13th harmonics, while the active filter is operated to compensate for any harmonics generated by the first unit and the rest of higher order harmonics of the load that are not compensated by the first unit. Both the units are connected to the same dc link that is maintained by the first unit. The proposed configuration is optimal in the sense that it uses only two passive filters to eliminate most of the lower order harmonics, while the two active filters take care of the remaining distortion. The critical parameters are given in Table I.
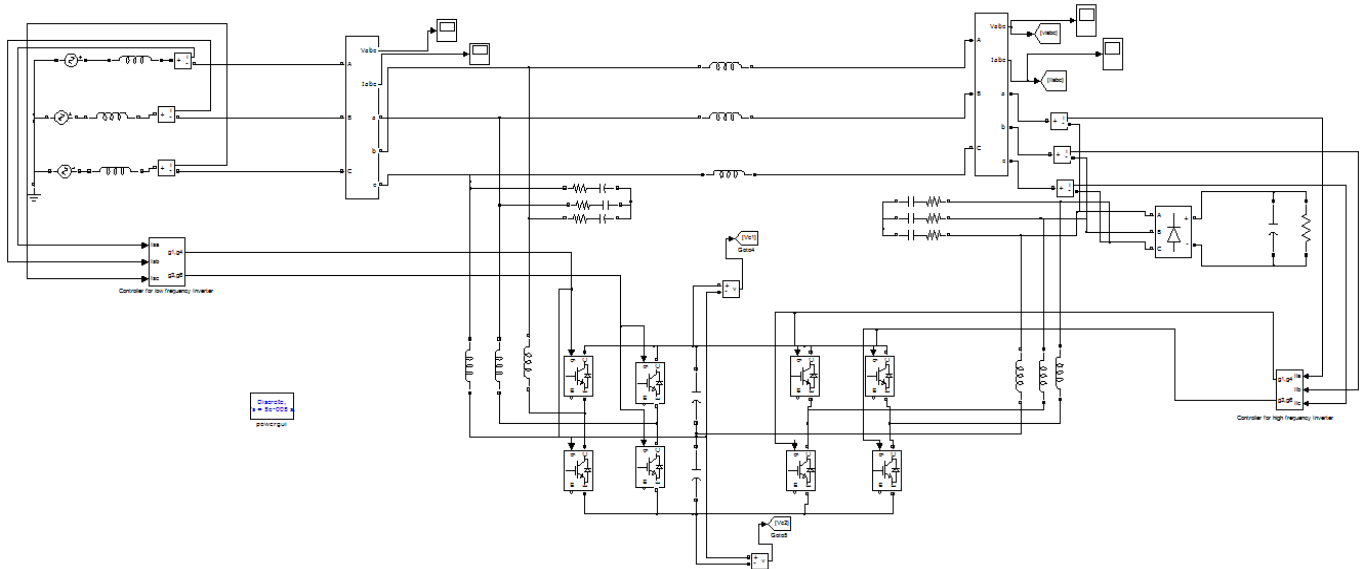
Fig.2.The proposed hybrid active power filter

III. THE PROPOSED HYBRID ACTIVE POWER FILTERS

The B4 bridges used as a hybrid active power filter are shown in Fig. 2**.** The reduction in the number of switches not only means a reduction in cost but also a reduction in the inverter losses. We define the variables $V_{sac} = V_{sa} - V_{sc}$, $i_{sac} = i_{sa} - i_{sc}$, $i_{Fac} = i_{Fa} - i_{Fc}$ and so on. Writing the KVL and KCL equations for the circuit under various switch conditions, the dynamics equations can be concisely expressed as a state space equation:

$$\frac{d}{dt}\begin{bmatrix} Li_{Fac}(t) \\ Li_{Fbc}(t) \\ V_{C1}(t) \\ V_{C2}(t) \end{bmatrix} = \mathbf{A}\begin{bmatrix} Li_{Fac}(t) \\ Li_{Fbc}(t) \\ V_{C1}(t) \\ V_{C2}(t) \end{bmatrix} + \mathbf{B}\begin{bmatrix} v_{Sac}(t) \\ v_{Sbc}(t) \end{bmatrix} \quad (1)$$

Where matrix A is a function of the switch states and B is a constant matrix. These are given in (2) and (3).

$$\mathbf{A} = \begin{bmatrix} 0 & 0 & -(1-s_a) & s_a \\ 0 & 0 & -(1-s_b) & s_b \\ k(1-2s_a+s_b) & k(1-2s_b+s_a) & 0 & 0 \\ k(-2s_a+s_b) & k(-2s_b+s_a) & 0 & 0 \end{bmatrix} \quad (2)$$

where $k = 1/3LC$.

$$\mathbf{B} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \quad (3)$$

In (2). Sa denotes the state of the bottom switch in the 'a' leg of the bridge and Sb that in the 'b' leg; Sa = 1 implies S1 is off and S4 is on while Sa = 0 implies S1 is on and S4is off. Similarly for the 'b' leg. It may be noted that the behaviour of the variable $iFac$ is shaped entirely by Sa and the variable $iFbc$ is shaped by Sb. When the top switch of a leg is on, the corresponding current decreases; and when the bottom switch of a leg is on, the corresponding current increases.

For complete current controllability, a one-one correspondence between the four possible switch states and the four possible combinations of changes in currents $iFac$ and $iFbc$ must be maintained. For this the capacitor voltages should individually exceed the line-line voltage at all times. This is a general control requirement of the **B4** topology. This means that the total DC voltage has to exceed twice the peak of the line-line voltage at all times. This is a disadvantage of the **B4** bridge because the high DC voltage entails higher device stress and higher switching losses per device. For this system the only quantities are the source and load line currents and voltages of the two dc side capacitors.

A. Control Equations

The one-cycle control equations for the filter may be derived in a manner similar to that given in [4]**.** Since the switching frequency is much higher than the line frequency, the inductor currents do not change much over one switching cycle. Hence net $iFac$ and $iFbc$ over Ts, is zero. Hence averaging (1):

$$Li_{Fac}(avg) = -V_{C1}(1-\delta_a) + V_{C2}\delta_a + V_{Sac} = 0 \quad (4)$$

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$$Li_{Fbc}(avg) = -V_{C1}(1-\delta_b) + V_{C2}\delta_b + V_{Sbc} = 0 \qquad (5)$$

For unity power factor operation, the source currents are in phase with the phase-neutral voltages. Thus, VSac = *v*sa-*vsc* = *Risa. - Risc = Risac* and *VSbc = Risbc* where *R* is the resistive load to be emulated. Using these and (4), (5)

$$Ri_{sac} = V_{c1} - (V_{c1} + V_{c2})\delta_a \qquad (6)$$

$$Ri_{sac} = V_{c1} - (V_{c1} + V_{c2})\delta_b \qquad (7)$$

Let Rs be the resistor used for sensing the values of *isa, isb* and *isc*. Then if Vm5 is *Rs/R* times VC, and Vm2 is *Rs/R* times Vc2, then the control equations become

$$R_s i_{sac} = V_{m1} - (V_{m1} + V_{m2})\delta_a \qquad (8)$$

$$R_s i_{sac} = V_{m1} - (V_{m1} + V_{m2})\delta_b \qquad (9)$$

B.   Operation

Fig.3. Controller for hybrid active power filter

The control of the bridge is such that the DC voltage is maintained constant. This is done by PI controllers and ensures that the bridge processes no active power. The terms Vm1 and Vm2, of (8) and (9) are obtained as the outputs of a PI controller to which the difference of the respective sensed capacitor voltage and a reference value is fed as input. The terms on the LHS of (8) and (9) are the voltages induced across the resistors used with the current sensors. Further, the control circuit requires a reset integrator and two comparators.

The bridge is operated at a constant switching frequency; *T,* is fixed. At the start of each cycle, switches S4 and S6

are closed, S1 and S3 are open; *SaSb* = 11. The integrator output is set to 0 (it is reset). The values *Rsisac* and Vm1 - l/Ts ∫ (Vm1 + Vm2) *dr* are compared and the output is the switch signal for the 'a' leg. When the two quantities become equal, the 'a' leg switch is toggled; thus the

control equation (8) is obeyed. Similarly the 'b' leg switch is controlled. Thus, after time *δaTs* switches S1 and S4 toggle and after time δbTs switches *S3* and S6 toggle. If at that time instant *δa (t) > δb(t),* the bridge will periodically (period = *Ts)* go through the switch states 11- 10 - 00 - 11. . . ; if instead at that time instant *δa(t) < δb (t),* the bridge will periodically go through the switch states 11- 01 -00 - 11 . . .

Here two controller circuits are used. One is for low frequency inverter and other is for high frequency inverter. For low frequency inverter source currents are taken as the input to the controller and for high frequency inverter load current are taken as the input to the controller.

IV. SIMULATION RESULTS

Fig.2. shows the MATLAB model of the hybrid active power filter. . The simulation is carried out in discrete mode at 5*10-5 step size with ode45 (Dormand-Prince) solver.
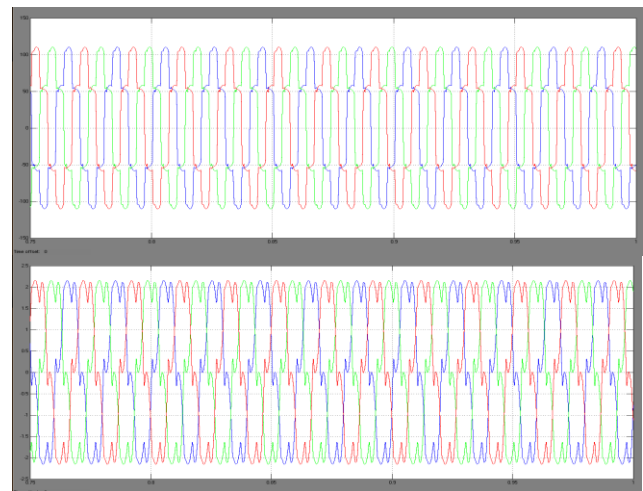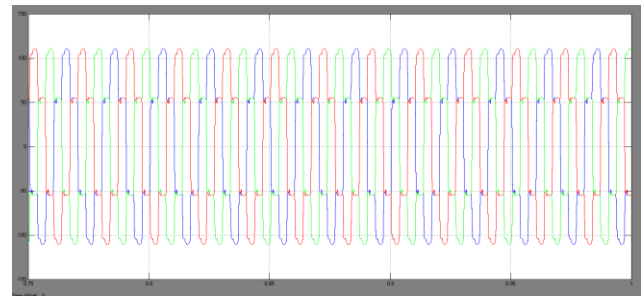

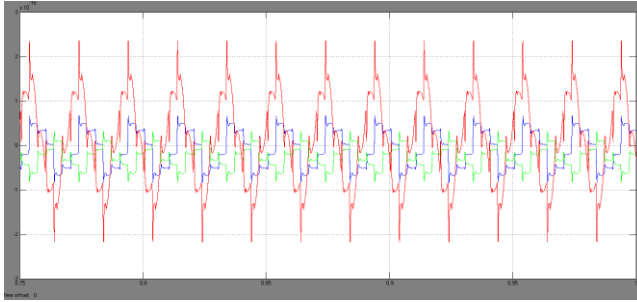Fig.4. source voltage and source current before connecting hybrid active power filter

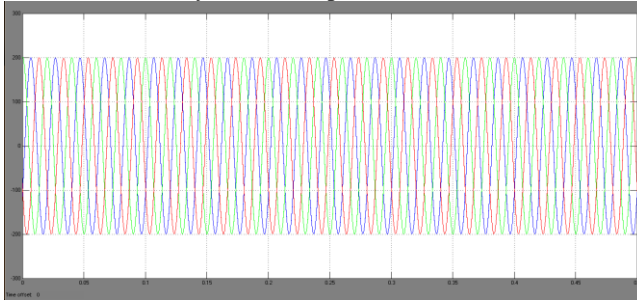Fig.5.Load voltage and load current before connecting hybrid active power filter

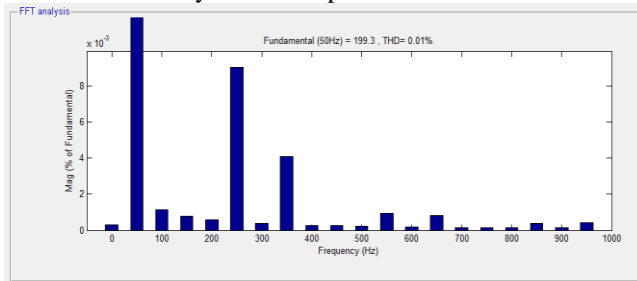Fig.6.Source Voltage and source current after connecting hybrid active power filter

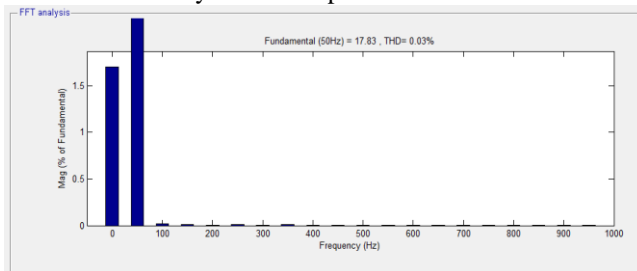Fig.7.THD analysis of source voltage after connecting hybrid active power filter

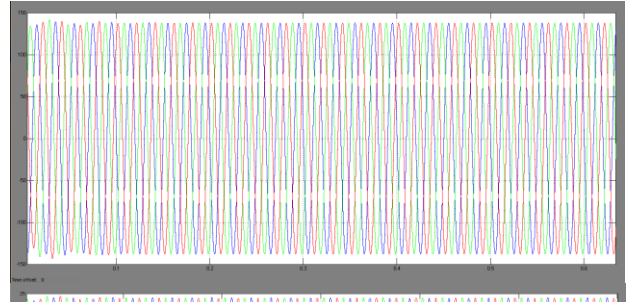Fig.8.THD analysis of source current after connecting hybrid active power filter

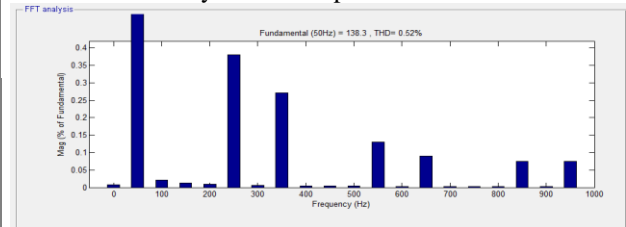Fig.9.Load voltage and load current after connecting hybrid active power filter

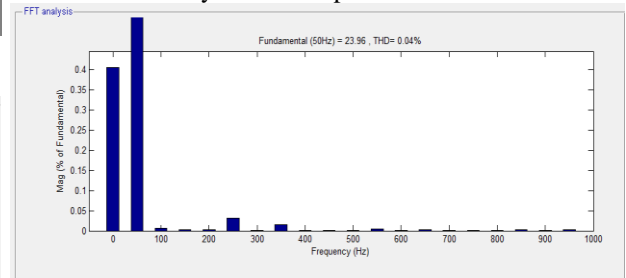Fig.10.THD analysis of load voltage after connecting hybrid active power filter

Fig.11.THD analysis of load current after connecting hybrid active power filter

In simulation studies, the results are specified before and after hybrid active power filter system are operated. The proposed control method has been examined under non-ideal mains voltage and unbalanced load current conditions. Before harmonic compensation the THD of the supply voltage is 27.93%. The obtained results show that the proposed control technique allows 0.5% mitigation of all harmonic components. The source current before compensation have a THD of 21% and after compensation it is reduced to 0.03%. The THD of load voltage before compensation is 27.93% and after compensation it is reduced to 0.52%. For load current before compensation the THD value is infinity and after compensation it is reduced to 0.04%.

V. CONCLUSION

This paper has proposed a hybrid dual inverter topology to operate as an APF. Two inverters operate in parallel and at different switching frequency. Each inverter is connected in series with a passive filter. The passive filter forthe LFI is designed to optimally eliminate fifth- and seventh-order harmonics, whereas the passive filter connected in series with the HFI is designed to optimally eliminate 11th- and 13th-order harmonics. The LFI operates typically around 550 Hz and takes care of only the lower order harmonics including reactive power demand of the system. The HFI operates typically around 20 kHz and makes the source current to adhere to the IEEE519 standard.

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